Application Note –1

Battery Pack Assembly Sequence and Connections Technique

Scope

This application note describes a recommended battery pack assembly sequence and connections technique between the battery pack and the PCB board for OZ890 application.

Description

OZ890 supports 5~13 series Li-ion battery pack, with integrated 13-channel ADC (13bit) for cell voltage measurement.

A 13 series battery pack application is shown in **Fig.1**. Optimizing the connection for cell voltage measurement channel can improve the accuracy of measurement for the lowest cell1 and the highest cell13. For cell voltage measurements, trace voltage drops for high current will reduce the accuracy of the lowest cell1 and the highest cell13, as there is high voltage drop along high current traces on VBAT+ and GND. Separate BC0 and GND/BC13 and VBAT+ from high current ground/power path, connect BC0 to GND (high current ground) at the negative terminal of the lowest cell1. Connect BC13 to VBAT+ (high current power) at the positive terminal of the highest cell 13. This approach is depicted in **Fig.1.**

Fig.2 shows another connection between the battery pack and the PCB board. This approach reduces the accuracy of measurement of the lowest cell1 and the highest cell13 due to voltage drop along high current traces on VBAT+ and GND.

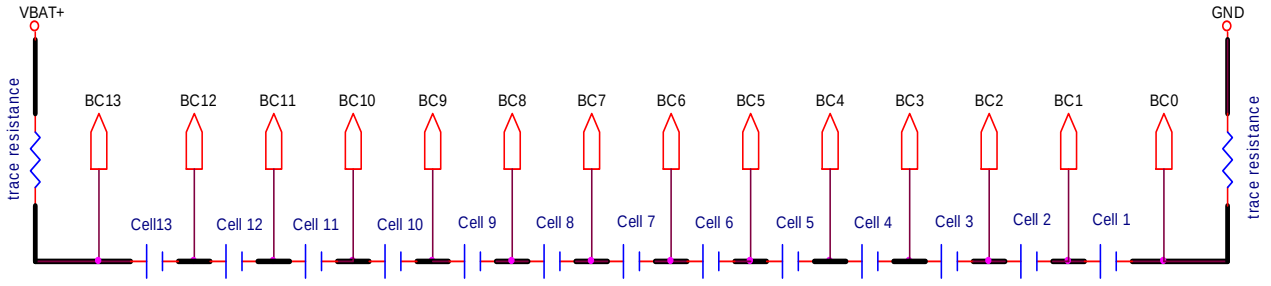

Figure 1

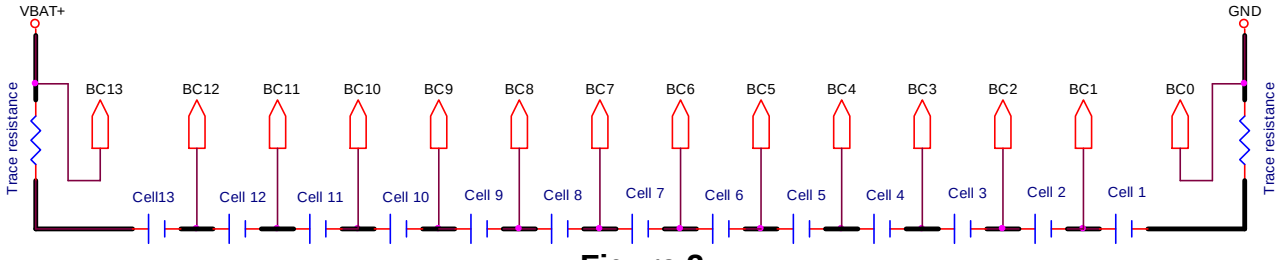

Figure 2

For 5,6,7,8,9,10,11,12 series Li-ion battery pack applications, the unconnected BC pads must be tied to the positive terminal of the highest cell. For example, in an 8 series Li-ion battery pack application, all BC9, BC10, BC11, BC12, BC13 must be tied to BC8 of the positive terminal of the highest cell8. This example is shown in Figure 3.

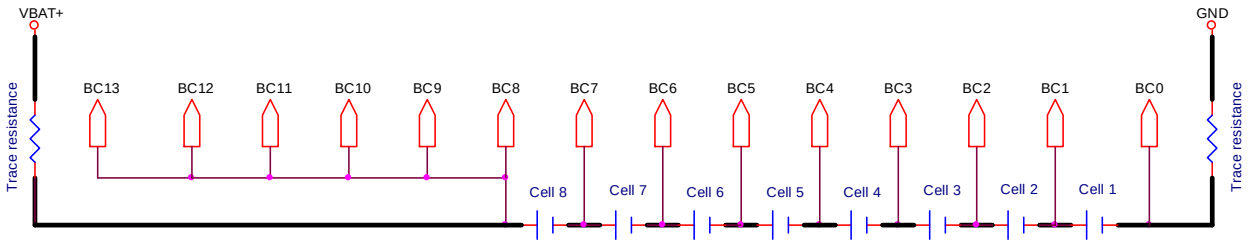

Figure 3

In order to maintain a low impedance ground/power connection back to the battery pack ground/power, it is usually necessary to use wide and short traces/wiring to reduce ground bounce and power bounce which are caused by the power/ground wire parasitic resistor and inductor, when the load current changes rapidly. The trace resistance between the negative terminal of the lowest cell1 and the GND of the board should be less than 5 mOhms at 300A short circuit high current for OZ890 chip application.

The final step of battery pack assembly is connecting cells to a PCB board with OZ890 protection and monitor chip.

The procedure must be performed in the following sequence:

1. **Connect GND and BC0 of board to negative terminal of lowest cell 1**
2. **Connect VBAT+ and BC13 of board to positive terminal of highest cell 13**
3. **Connect positive terminal of cell 1 to BC1 of board**
4. **Connect positive terminal of cell 2 to BC2 of board**
5. **Connect positive terminal of cell 3 to BC3 of board**
6. **Connect positive terminal of cell 4 to BC4 of board**
7. **Connect positive terminal of cell 5 to BC5 of board**
8. **Connect positive terminal of cell 6 to BC6 of board**
9. **Connect positive terminal of cell 7 to BC7 of board**
10. **Connect positive terminal of cell 8 to BC8 of board**
11. **Connect positive terminal of cell 9 to BC9 of board**
12. **Connect positive terminal of cell 10 to BC10 of board**
13. **Connect positive terminal of cell 11 to BC11 of board**
14. **Connect positive terminal of cell 12 to BC12 of board**

After the cells have been connected to the PCB board, sOZ890 will start up only after one low pulse of RSTN pin is detected.
Note: To ensure system reliability after cell assembly, after OZ890 battery assembly and power up, please set bit 5 “rstn_bypass” in EE register 32h to “1”. This ensures that the OZ890 can start up without one low pulse of RSTN. Setting this bit lets OZ890 know

the difference between a power-up event after assembly versus a power-up event after deep discharge. The description of bit 5 in EE register 32h is as shown below:

EE Register 32h

Bit #	Name	Description	R/W	Reset Value
5	rstn_bypass	This bit is used to control the rstn low pulse check function. If “0”, the rstn low pulse check is needed, the chip will not scan until the rstn low pulse is checked; if “1”, the rstn low pulse check is ignored, the chip will scan no matter whether the rstn low pulse is checked or not. After battery assembly, this bit should be mapped as “1” from the EEPROM data.	RW	0h

Application Note –2
Using the 4–Wire I²C Communication Interface

Scope
This application note describes the use of the OZ890 4-wire I²C communication interface.

Description
OZ890 has an I²C bus used for communication. It can operate in special 4-wire mode. The 4-wire mode is useful for electrically isolated communication.

In some non-common ground and/or high noise application, the Opto-coupler should be employed to electrically isolate the I²C bus [1]. Referring to Figure 1, the 4-wire mode is suitable for a low cost implementation of an optically coupled, electrically isolated communication.

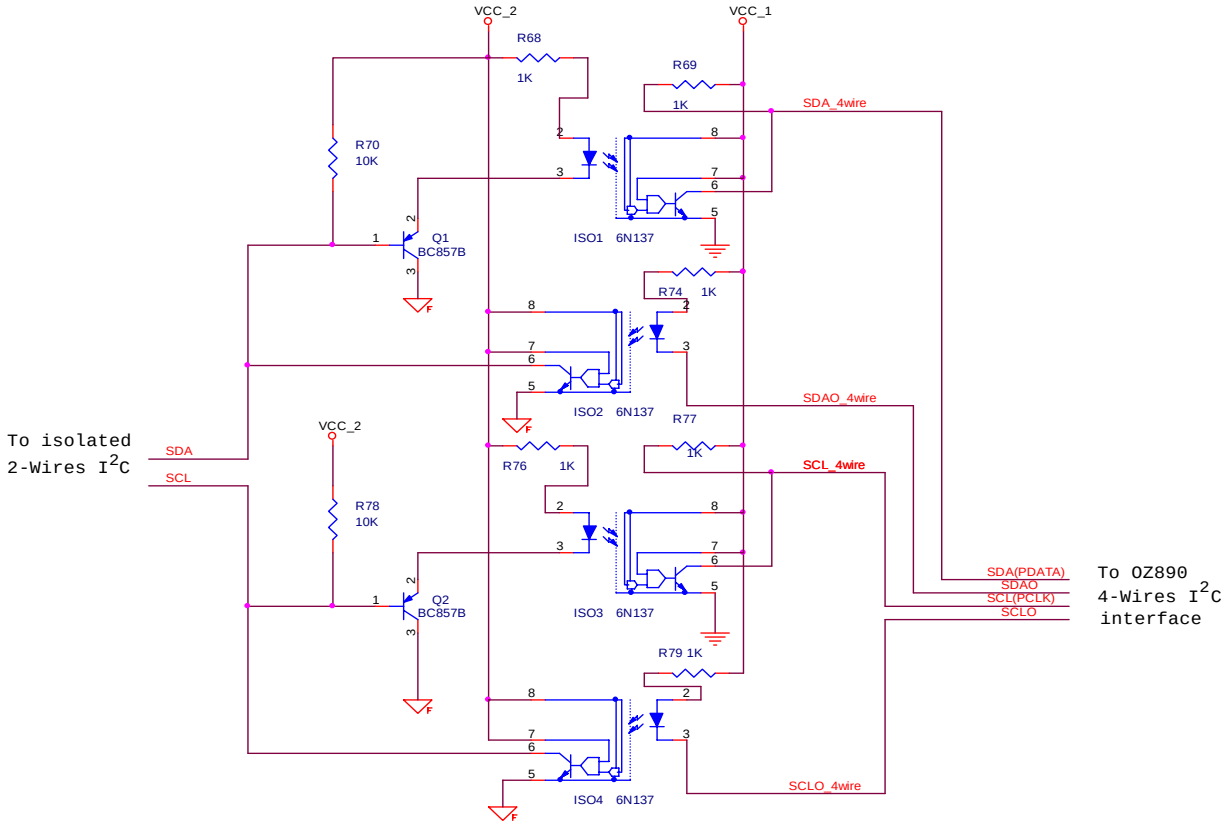

Figure1. 4-wires I²C isolated application

Referring to the OZ890 datasheet, to enter the 4-wire mode, OZ890 must be set in software mode, 'BSEL1' held at '0' and 'BSEL0' held at '1'.

Table1. OZ890 Pin Description

Name	Pin No	I/O	Pin Type	Application Description	
				Hardware Mode	Software Mode
BSEL1	30	I	Digital	Bus type configure input1	
BSEL0	31	I	Digital	Bus type configure input0	
LED1/SCLO	25	I/O	Digital	Led driver	4 wire I2C clock output
SCL (PCLK)	26	I/O	Digital	I2C (PBUS) clock line	I2C (PBUS) clock line/4wire I2C clock input
LED0/SDAO	27	I/O	Digital	Led driver	4 wire I2C data output
SDA (PDATA)	28	I/O	Digital	I2C (PBUS) data line	I2C (PBUS) data line/4 wire I2C data input

Reference

1. *Method provides fast, glitch-free isolation of I2C and SMBus signals*, Mark Thoren, Linear Technology Corp, Milpitas, CA -- EDN, 6/24/2004

Appendix A: 4-wire I²C mode demo program in C

```
/* 4-wire IIC c demo */
#define DELAY (_nop_();_nop_();_nop_();_nop_();)


  void IIC_Start(void)
  {
     SDAO=1;
     DELAY;
     SCLO=1;
     DELAY; DELAY;
     SDAO=0;
     DELAY; DELAY;
     SCLO=0;
     DELAY;
  }

  void IIC_Stop(void)
  {
     SDAO=0;
     DELAY;
     SCLO=1;
```

```
    DELAY; DELAY;
    SDAO=1;
    DELAY; DELAY;
}

void SEND_0(void)
{
    SDAO=0;
    DELAY;
    SCLO=1;
    DELAY; DELAY;
    SCLO=0;
    DELAY; DELAY;
}

void SEND_1(void)
{
    SDAO=1;
    DELAY;
    SCLO=1;
    DELAY; DELAY;
    SCLO=0;
    DELAY; DELAY;
}

bit Check_Acknowledge(void)
{
      bit FLAG;

    SDAO=1;
    DELAY;
    SCLO=1;
    DELAY;
    FLAG=SDA;
    DELAY;
    SCLO=0;
    DELAY;
    if(FLAG==1)
       return FALSE;
    return TRUE;
}

void Write_Byte(uchar b)
{
```

```
    uchar i;

    for(i=0;i<8;i++)
    {
        if((b<<i)&0x80)
            SEND_1();
        else
            SEND_0();
        }
}

bit Write_N_Bytes(uchar *buffer,uchar n)
{
    uchar i;

    IIC_Start();
    for(i=0;i<n;i++)
    {
        Write_Byte(buffer[i]);
        if(!Check_Acknowledge())
        {
            IIC_Stop();
            return(i==n);
            }
    }
    IIC_Stop();
    return TRUE;
}

uchar Read_Byte(void)
{
    uchar b=0,i;
      bit FLAG;

    for(i=0;i<8;i++)
    {
        SDAO=1;
        SCLO=1;
        DELAY;DELAY;
        DELAY;DELAY;
        FLAG=SDA;
        DELAY;DELAY;
        DELAY;DELAY;
        SCLO=0;
```

```
        if(FLAG==1)
           {
              b=b<<1;
              b=b|0x01;
           }
        else
           b=b<<1;
    }
    return b;
}

bit Read_N_Bytes(uchar SlaveAdr,uchar n,uchar *buffer)
{
    uchar i;

    IIC_Start();
    Write_Byte(SlaveAdr);
    if(!Check_Acknowledge())
       return FALSE;
    for(i=0;i<n;i++)
       {
          buffer[i]=Read_Byte();
          if(i!=n)
             SEND_0();
          else
             SEND_1();
       }
    IIC_Stop();
    return TRUE;
}
```

Application Note –7

OZ890 functions in multi-OZ890 system

Scope

This application note describes the functions of multiple OZ890 chips in a battery management system. The multi-OZ890 battery management system is used to monitor and manage the multi-cell battery pack where the number of cells is more than 13. The system can be designed for the EM (Electric Motor), EV (Electric Vehicle), HEV (Hybrid Electric Vehicle) and UPS applications.

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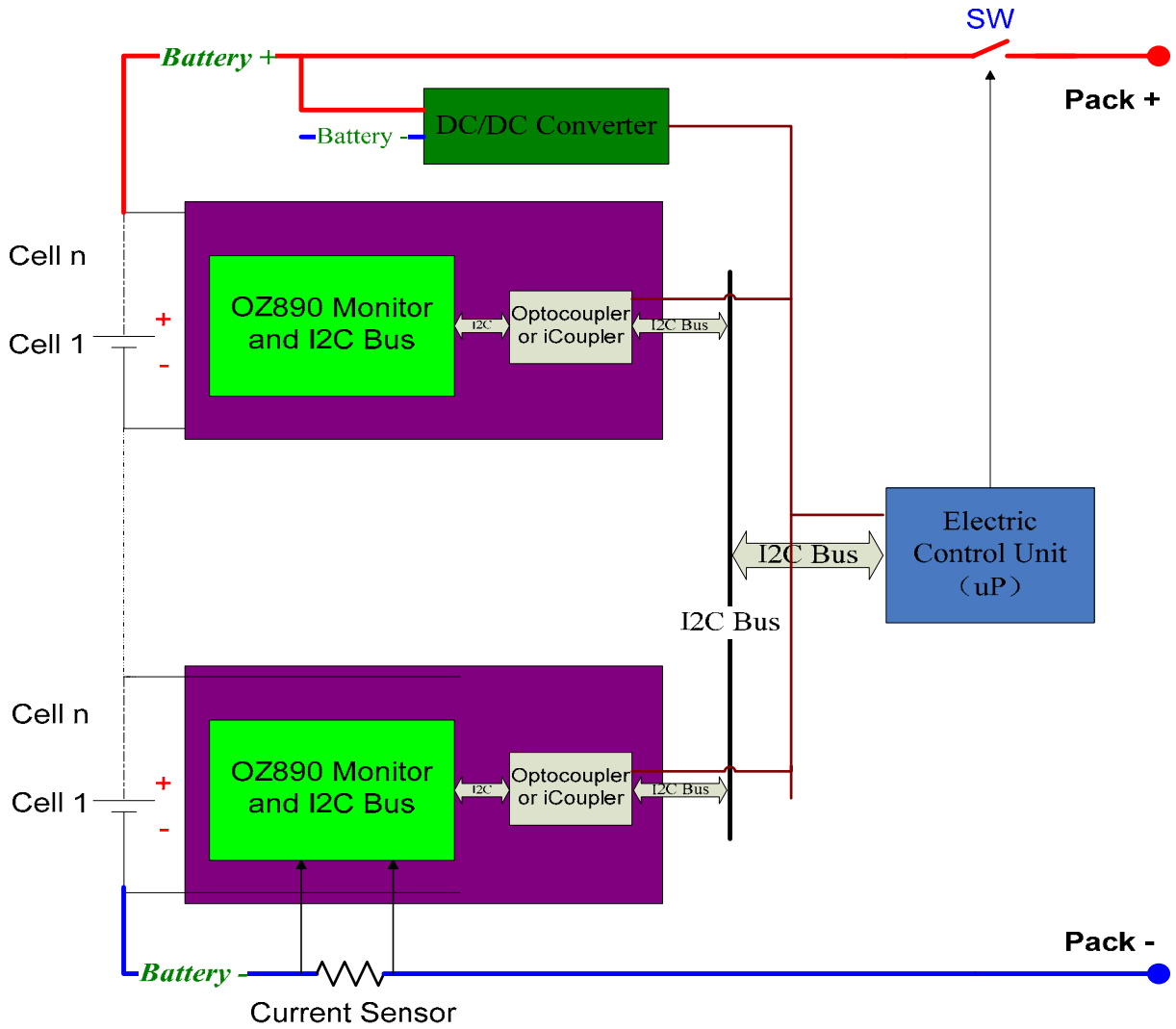
Description

Figure 1. Connection for multiple OZ890s



In the multi-OZ890 battery management system OZ890 acts as a slave device, OZ890 must work in the Software Mode (please check the software mode application note AN-6). The uP collects data and event information via the I^2C Bus from OZ890. With this information, the SW carries out gas gauge calculation or takes other appropriate actions.

In the multi-OZ890 battery management system OZ890 works in software mode in which many functions can be controlled by the uP. Setting OZ890's EE register 32h to 0, selects the software mode. When register 32h is set to 1, OZ890 works in the hardware mode.

In the multi-OZ890 battery management system, OZ890's role is to collect and transfer the cell data, inform the event to the uP, and support the following functions:

- **Voltage measurement**
- **Temperature measurement**
- **Current measurement**
- **Balance function**
- **Protection signal**
- **Disconnect detection**
- **ADC calibration**
- **I^2C communication**
- **I^2C Address Configuration**

Voltage Measurement

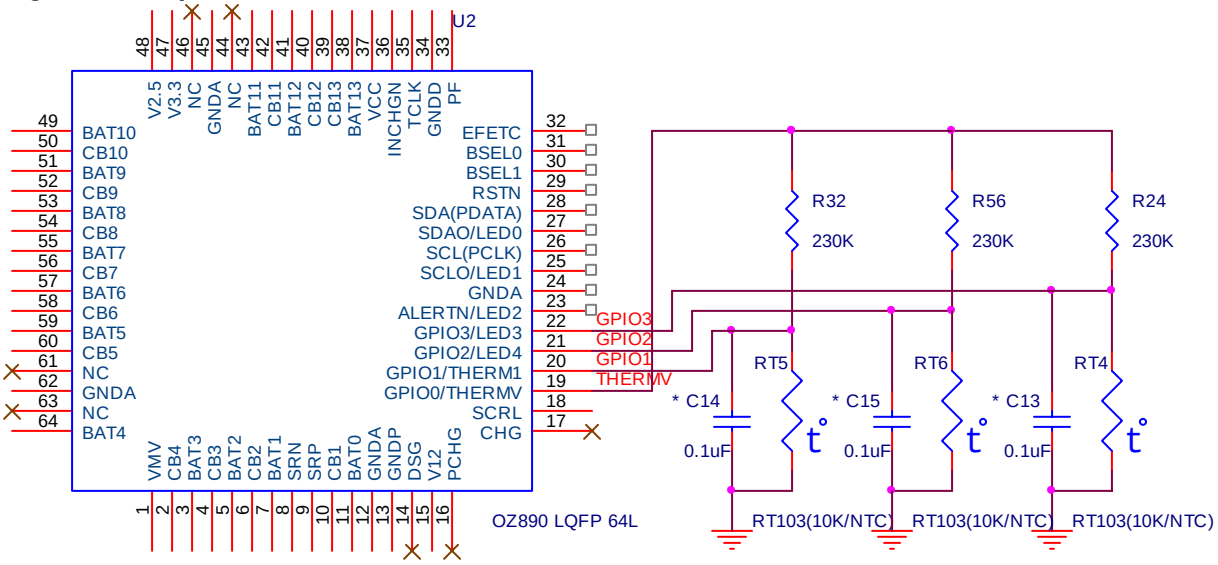
In the system each OZ890 has 5～13 channels for cell voltage measurement.
Resolution: 13bits (signed), the measured error can be within ±15mV
Input Voltage Range: -0.3V~5.0V
Auto offset cancellation.
Slope calibration can be implemented by the uP for better accuracy

Temperature Measurement

OZ890 has embedded an internal temperature sensor that is for internal temperature measurement. There are 3 channels (GPIO1, GPIO2, and GPIO3) that can be configured for external temperature measurement, if GPIO1, GPIO2 and GPIO3 are set as 01. For detailed configuration information please refer to operation register 2dh in the OZ890 datasheet.
Accuracy: 13bits (signed) the measured error can be within ±15mV
Input Voltage Range: 0.3V~2.5V
Auto offset cancellation.
Slope calibration can be implemented by the uP for better accuracy.

Please refer to figure 2.

Figure 2: temperature monitor



Current Measurement

In the multi-OZ890 system, as shown in figure 1, the lower OZ890 chip's ADC current channel can be used to measure current directly. GPIO3 can be connected to current transducer to monitor the system current. The accuracy of GPIO3 is programmable to be 13-16 bits in the registers; this channel can also be used as a current measurement channel.

OZ890 chip's ADC current channel is a dedicated channel to measure the current across the sense resistor (0.1mΩ to 15.5mΩ) during charging and discharging for coulomb counting or other purpose.

Resolution: 16-bit (signed)
Input Voltage Range: ±250mV
Auto offset cancellation
Slope calibration can be implemented by the uP for better accuracy.

OZ890 can scan the voltage channel, temperature channel and current channel in 1 second. It takes 25% of the cycle to measure the current. An ADC ***request function*** is needed if you want to increase the current measure time to be 50% of the scan cycle (please check the software application note AN-6). Compensation is needed while calculating the coulomb counting based on the current measured by OZ890, since the current measurement does not use the full scan cycle.

Balance Function

In the system, the OZ890 can do cell balance at any time as controlled by the uP. According to collected cell voltage data from each OZ890, the uP decides which cell needs bleeding.

The uP controls each OZ890 operation 22h & 23h registers and some bleeding parameters, to enable bleeding. Set the *Bleeding_enable(bit5)* to "1".

22h: *bleeding_cell's_low_byte*(bit7-0): corresponding to the cell8~cell1 respectively for the cell bleeding

23h: *bleeding_cell's_high_byte*(bit4-0): corresponding to the cell9~cell13 respectively for the cell bleeding

bleeding_enable(bit5): used to enable/disable the bleeding

Once cell bleed has been turned on, it remains active until the uP turns it off.

Note: During cell bleeding, if the OZ890 detects some error such as OV, UV, OC, SC, OT, UT, the cell bleeding will be stopped right away; only when the fault condition is released, cell bleeding becomes active.

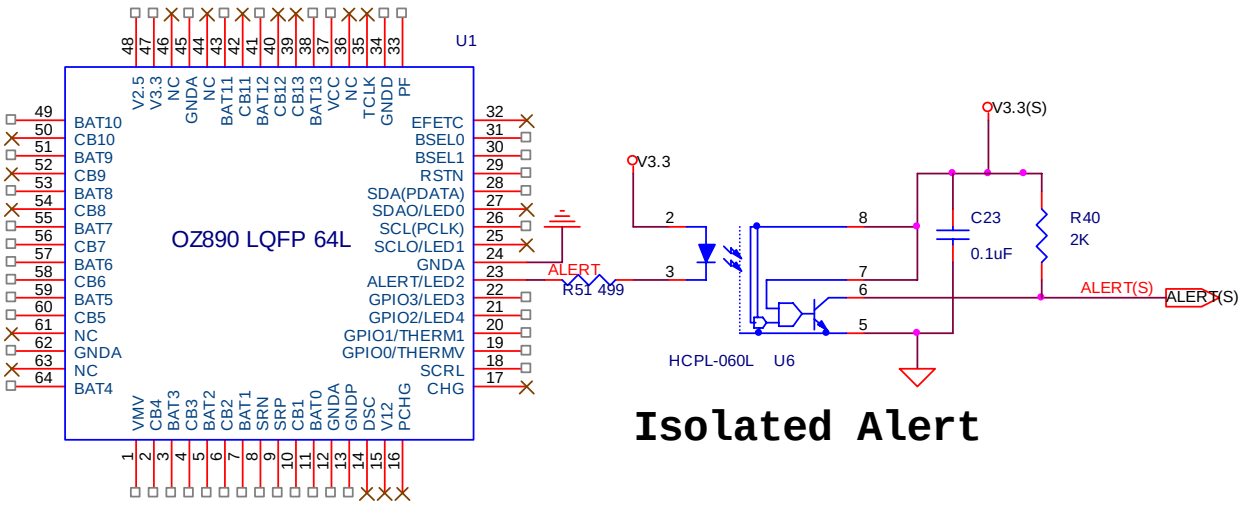
Protection Control

a) Alert_n Error Signal

OZ890 provides an exclusive pin Alert to send the interrupt signal to the uP when error condition such as ADC event, GPIO event, OV, UV, OC, SC, OT, UT, MOSFET fail event, PFVH event, or PFVL event occurs. Any release action fully relies on the uP's decision. Please refer to event enable register 2ah.

In multi-OZ890 battery management system, use an opto-coupler to transfer ALERT signal because each chip has non-common ground. Please refer to figure 3.

Figure 3: alert signal transfer



b) OC Event Control

In the multi-OZ890 system, use lower OZ890 ADC current channel to monitor system current. It can signal OC event signal in its operation register 2bh. And the charge and discharge over-current thresholds (***CHGOverCurrentTH*** and ***DSGOverCurrentTH***) are set in EEPROM registers 28h and 29h. (Also define the discharge current threshold in EE register 28h; define the charge current threshold in EE register 29h to determine if the system is in charge or discharge state.) The delay time can be programmed from 2ms to 16.3sec by the parameter ***OverCurrentDelay*** in EEPROM register 2ah.

Charge Voc: 10mV to 105mV, in 5mV steps.
Discharge Voc: 30mV to 285mV, in 5mV steps.

c) SC Event Control

In the multi-OZ890 system lower OZ890 ADC current channel monitors system current. It can sign SC event signal in operation register 2bh. Bits [5:0] in EE register 2bh are to configure the short circuit threshold. Short circuit detection is very similar to over-current detection. Short circuit threshold Vsc can be programmed from 50mV to 620mV (10mV each step) by the parameter ***ShortCurrentTH*** in EEPROM register 2bh. Short circuit delay time can be programmed from 4us to 32.6ms. It is configured by EEPROM register 2ch by the parameter ***ShortCurrentDelay***.

d) OV/UV Event Control

In the system according to cell voltage data from each OZ890, the uP can do OV/UV event control.
Also each OZ890 can do OV/UV event control and sign the event signal. Set ***OverVoltageTH*** in EE register 4ah and 4bh; set ***UNderVoltageTH*** in 4eh and 4fh. Then sign OV/UV event signal in operation register 2bh. UV/OV delay time can be in EEPROM register 2eh, Bit3-Bit0.

e) OT/UT Event Control

In multi-OZ890 system GPIO1, GPIO2 and GPIO3 can each do thermal monitoring. According to temperature data from each chip, the uP can do UT/OT event control. Also, each OZ890 can do UT/OT event control. Set ***ExtOverTempTH*** in EE register 56h and 57h; set ***IntOverTempTH*** in EE 5eh and 5fh; set ***ExtUnderTempTH*** in EE register 5ah and 5bh; set ***IntUnderTempTH*** in EE register 62h and 63h. If each OZ890 detect the temperature is above the threshold ***ExtOverTempTH*** or ***IntOverTempTH,*** it will sign OT event signal in operation register 2bh. If OZ890 detects the temperature is lower than ***ExtUnderTempTH*** or ***IntUnderTempTH***, it will sign the UT event signal in operation register 2bh.
External and operation OT/UT delay time can be programmed in EEPROM register 2eh, Bit7-Bit4.

f) PF Cell Unbalance Check

In multi-OZ890 system if each OZ890 chip once detects the cell unbalance, it will make ALERT active to inform the uP. Then the uP can query the corresponding event register 15h to check if unbalance event has occurred or not.

g) PFVH/PFVL check

In multi-OZ890 system if each OZ890 once detects cell voltage is over PFVH threshold or lower than PFVL threshold, it will signal ALERT active to inform the uP. Then the uP can query the corresponding event register 15h to check if PFVH/PFVL event has occurred or not.

Disconnection Detection

OZ890 chip provides the disconnection detection function which can be used to check the disconnection between the battery ends and the OZ890 ADC input pins. The uP can set OZ890 disconnection_detection register bits in operation register 31h. If these bits are set to “101”, when cell voltage is converted to digital, cell bleeding is enabled (bleeding cell voltage is measured); if these bits are set to “000”, when ADC is performed on the cell voltage, the cell bleeding is disabled (normal cell voltage is measured).

The disconnection detection function relies on the uP to make judgment and decision. According to the cell voltage data from OZ890, the uP searches for the max_voltage, among the cells. Then it compares other cell voltages with the max voltage. If the max_voltage – the cell voltage > set value (which will be set in the uP, and judged by the uP.), the cell will be regarded as disconnected; otherwise, the cell will be regarded as a normal connection.

ADC calibration

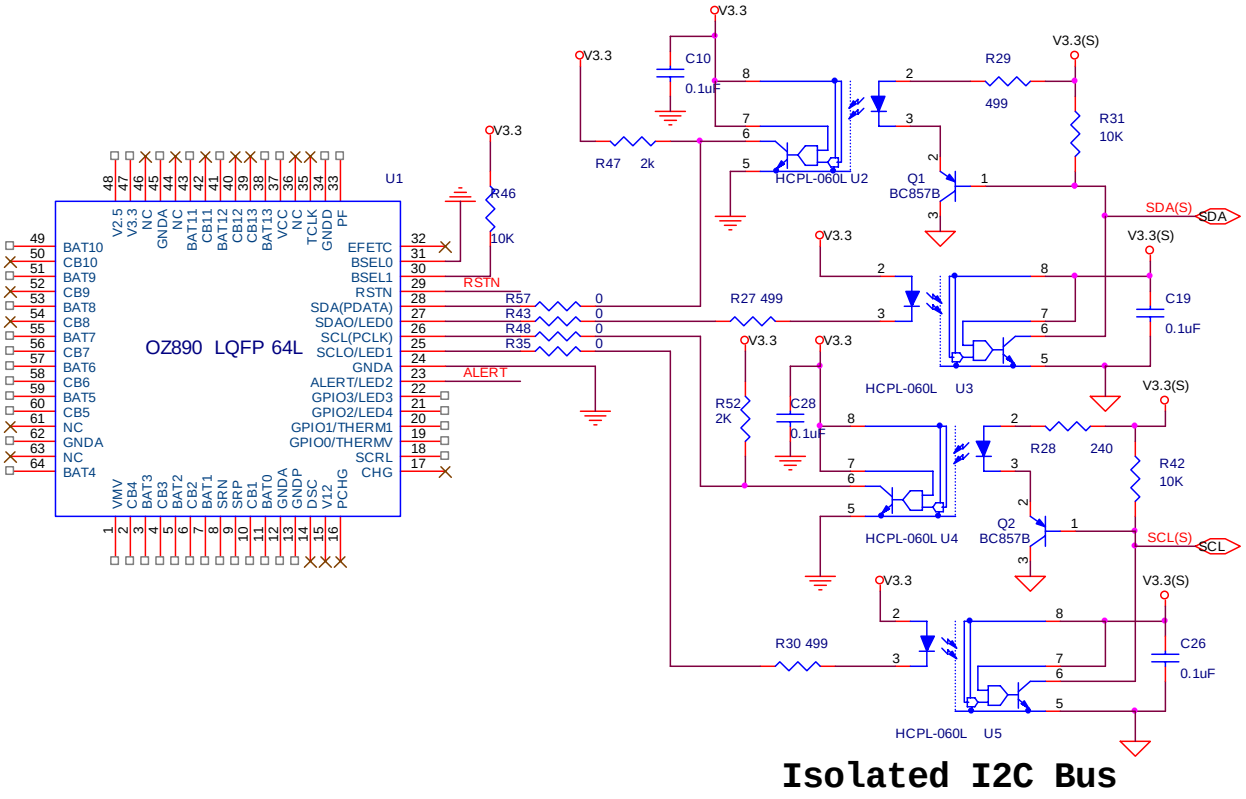
In multi-OZ890 system if there is a need to improve precision of voltage, current, temperature measurement, the uP can do offset calibration and slope calibration for ADCs on the related channels. For details please refer to ADC request and ADC calibration in application note OZ890 AN-8.

I^2C Communication Bus

In multi-OZ890 system 4-wries I^2C Bus is recommended because all chips are non-common ground. 4-wire I2C bus is easy to use with external general-purpose opto-coupler.

In this case, Pin31 BSEL0 is connected to ground; Pin 32 SBEL1 is connected to 3.3V. (bsel1, bsel0=10 is for 4-wire I^2C Bus.). Pin25 is the output clock pin (SCLO) and Pin26 is the input clock pin (SCL), Pin27 is the output data pin (SDAO), Pin28 is the input data pin (SDA). This Bus protocol and timing is the same as 2-wire I^2C bus except separating input/output line. Please refer to figure 4.

Figure 4: Isolated 4-wire I²C Bus



I²C Address Configuration

In multi-OZ890 system the Electric control unit (uP) communicates with each OZ890 via a unique I²C address. The OZ890 I²C address is set by the EEPROM register 30h Bit3-Bit0.

OZ890 EEPROM register 30h:

Address	Bit3	Bit2	Bit1	Bit0
30h	I²C Addr3	I²C Addr2	I²C Addr1	I²C Addr0

Bit3 – Bit0 (I²C Addr3 – I²C Addr0): Configure the I²C address.
The I²C address = 60h (7 bits) +2N (N: 0~15).

Application Note –11

Application circuits for 5~13 cells Li-ion battery pack

Scope

This application note describes typical application circuits for 5S, 6S, 7S, 8S, 9S, 10S, 11S, 12S and 13S cells Li-ion battery pack.

Description

OZ890 supports 5~13 cells series Li-ion battery pack, For 5 cells series Li-ion battery pack application, the following steps and application schematic shown in **Fig.1** are recommended:

- **The unconnected BAT6, BAT7, BAT8, BAT9, BAT10, BAT11, BAT12, BAT13 pins of OZ890 must be tied to BC5 of the positive terminal of the highest cell 5 by 510 ohms resistor as in Fig.1.**
- **Separated BC0 to GND, BC5 to VBAT+ connection for cell1 and cell5 measurement accuracy as in Fig.1.**

5 cells series battery pack application is shown in **Fig.1.**

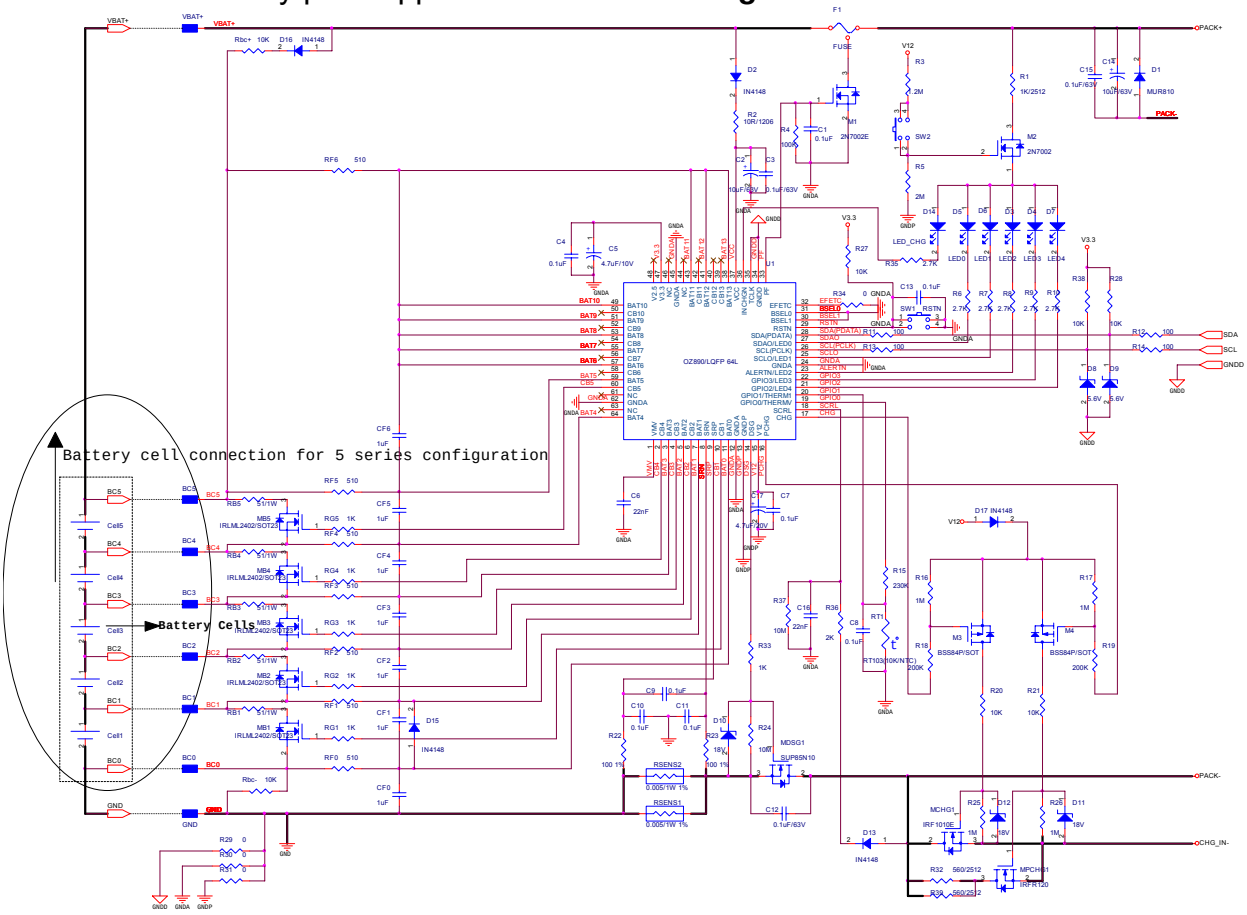


Fig.1 — 5 cells series application

Application Note –13

Cell Balance Implementation in Software Mode

Overview

To keep the balance among battery cells, OZ890 software mode supports cell bleeding of Li-ion batteries when they are being charged. OZ890 does not support cell bleeding for NiMH batteries in any conditions. In software mode, OZ890 can balance the cells at anytime under the control of uP.

If the bleeding is enabled in idle state, during cell bleeding, if the safety check logic detects some error such as OV, UV, OC, SC, OT, UT, the cell bleeding will be stopped right away; also if the bleeding is disabled in idle state, during cell bleeding, if the chip is not in charge state or the safety check logic detects some error such as OV, UV, OC, SC, OT, UT, cell bleeding will be stopped right away.

Cell Balance Configuration

The related registers of OZ890 for cell balance are: internal register 22h and internal register 23h. Once cell bleeding has been turned on by software, it remains active until software turns it off or until an error condition takes place. These errors include over voltage, under voltage, over current, short circuit, over temperature, and under temperature.

Internal register 22h: Software Bleeding1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bleeding_Cell's low byte							

Bit [0-7]: There 8 bits correspond to the cell8~cell1 respectively for the software cell bleeding, for example, bit 7 is set to "1" to select cell 8 for bleeding; bit 0 is set to "1" to select cell 1 for bleeding.

Internal register 23: Software Bleeding2 Register

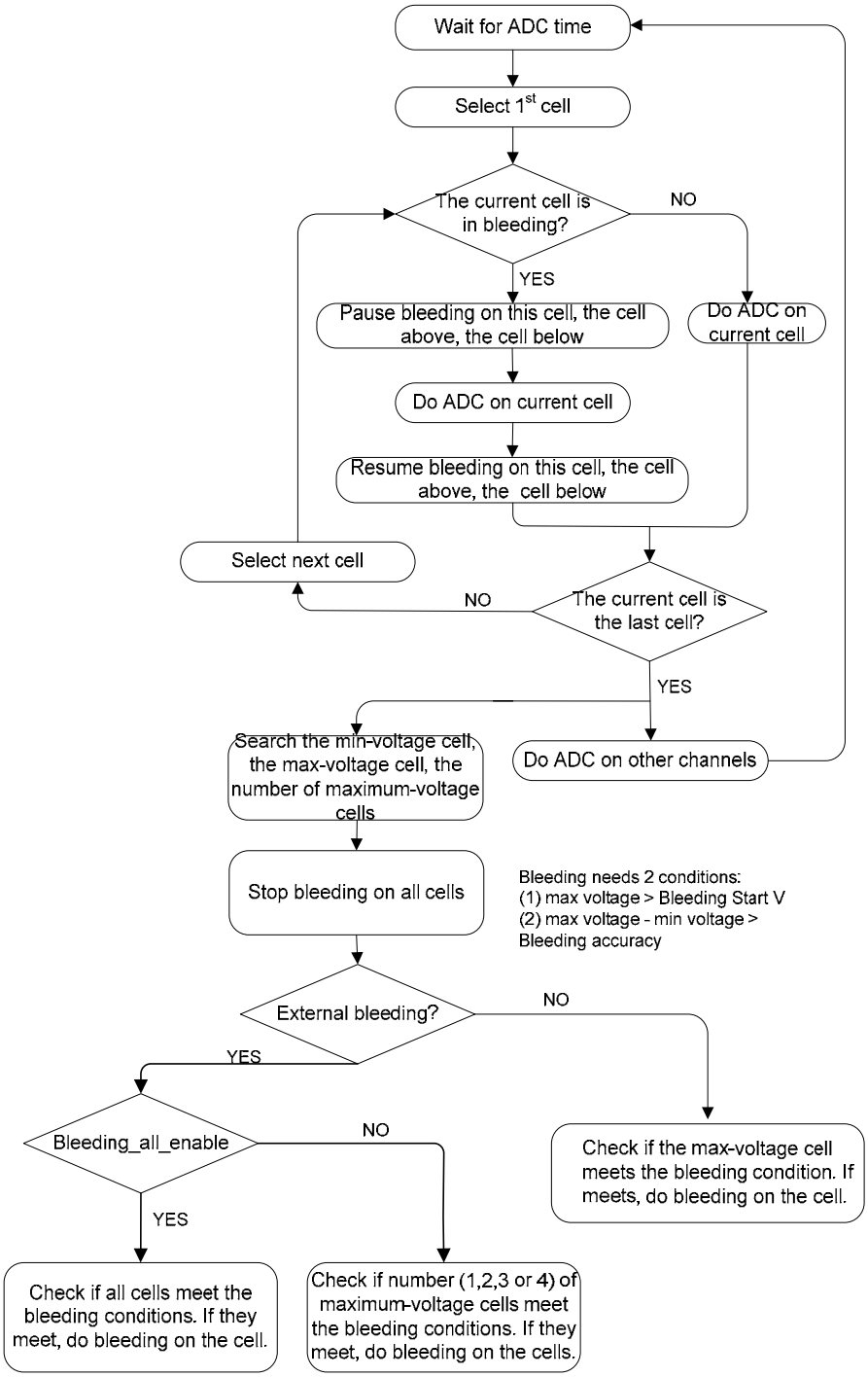
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tclk frequency		Bleeding enable	Bleeding_Cell's high byte				

Bit [0-4]: These 5 bits correspond to cell 13~cell 9 respectively for software cell bleeding, for example, bit 5 is set to "1" to select cell 13 for bleeding; bit 0 is set to "1" to select cell 1 for bleeding.

Bit [5]: This bit is used to enable software bleeding. If set to "1", it enables software bleeding; if set to "0", it disables software bleeding. In hardware mode, this bit is ignored.

Bit [6-7]: Skip

Cell Bleeding Control of OZ890 in software mode



Cell Bleeding Control Flow Diagram

Figure 1

Cell bleeding control is as follows:
(a) Wait for ADC time.
(b) Select the 1st cell.
(c) If the current cell is in bleeding, then pause bleeding on this cell, the cell above and the cell below.
(d) If the current cell is not the last cell, select the next cell, go to step (c); if the current cell is the last cell, go to step (e);
(e) Do bleeding check. At the same time, do ADC on other channels; after that go to step (a). For the bleeding check, do the following steps:
Search the min-voltage cell, max-voltage cell, then check the max-voltage cell to meet the bleeding condition (cell voltage > bleeding start point voltage; cell voltage –min voltage > the bleeding accuracy such as 10mv which is specified by the bleeding accuracy register bits)

for the external bleeding case and bleeding_all_enable = “0”, assuming the max bleeding cell number is N, search the N cells that meet the bleeding conditions in the order cell1, cell2, cell3, … The procedure is as follows:
(i) Find the N maximum-voltage cells
(ii) Stop the bleedings on all cells
(iii) Check if maximum-voltage cells meet the bleeding condition or not.
If the cell meets the condition, do bleeding on the cell.
If it does not meet the condition, do not bleed that cell.

For the external bleeding case and bleeding_all_enable = “1”,
(i) Stop bleedings on all cells
(ii) Check if all cells meet the bleeding condition or not.
If the cell meets the condition, do bleeding on the cell.
If it does not meet the condition, do not bleed that cell.

for the internal bleeding case, at first, stop bleeding on all cells, then check if the max-voltage cell meets the bleeding condition or not. If the cell meets the condition, do bleeding on the cell. If it does not meet the condition, do not bleed that cell

The flow chart of cell balance control is shown in figure 1.

Sample of C code

```
//This function search cells for bleeding
    for(i=0; i<cCellNumber; i++)
    {
        if ((MaxVoltage - *CellVol) <= cBleedAccuracy)
        {
            if (i <= 7)
                mask1 |= (0x01 << i) ;        // cell1 ~ cell8 bleeding mask
            else
                mask2 |= (0x01 << (i-8)) ;   // cell9 ~ cell13 bleeding mask

            bleed_cnt++ ;                    // bleeding counter
            Vol[i] = *CellVol ;      // save voltage values
        }

        *CellVol++ ;
    }


    // cell balance number check

    if (bleed_cnt > cBleedMaxNum)

    {

        for(i=0; i<cBleedMaxNum; i++)

        {

            min_vol = 9999 ;

            /* find min voltage cell number */

            for(j=0; j<cCellNumber; j++)

            {

                if(min_vol > Vol[j])

                {

                    min_vol = Vol[j] ;

                    Vol[j] = 9999 ;

                    idx = j ;
```

```
                        }
                }
                /* clear corresponding bleeding bit */
                if (idx <= 7)
                        mask1 &= ~(0x01 << idx) ; // cell1 ~ cell8 bleeding mask
                else
                        mask2 &= ~(0x01 << (idx-8)) ;// cell9 ~ cell13 bleeding mask
        }
}

// set bleeding1 register
HwPwrite(SW_BLEEDING1_ADDR, mask1) ;

// set bleeding 2 register & bleeding enable
HwPwrite(SW_BLEEDING2_ADDR, HwPread(SW_BLEEDING2_ADDR)|0x20|mask2) ;
```

Application Note –16

Application circuits for Dual OZ890 system (OZ890 works in hardware mode)

Scope

This application note describes typical application circuits for a battery management system with two OZ890s. In this system OZ890 works in hardware mode. The system design can be optimized for EM (Electric Motor) and UPS applications.

This application focuses on one type of implementation, for example 8+8 cells in series. Other implementations where the number of cells is anywhere from 14 to 25 could be based on this aforementioned implementation described in this application note.

Description

Figure1. The architecture of multi-OZ890 block

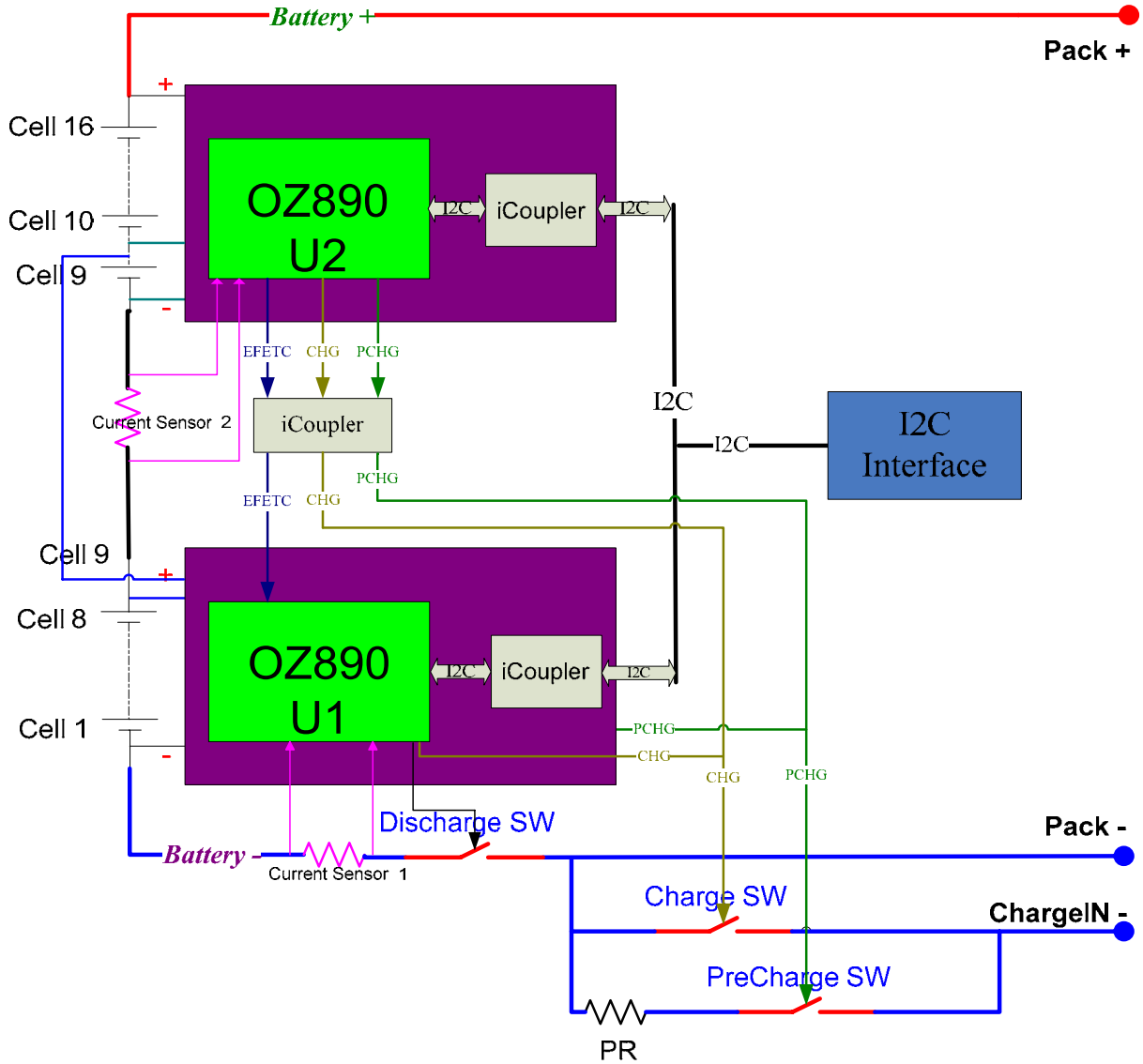
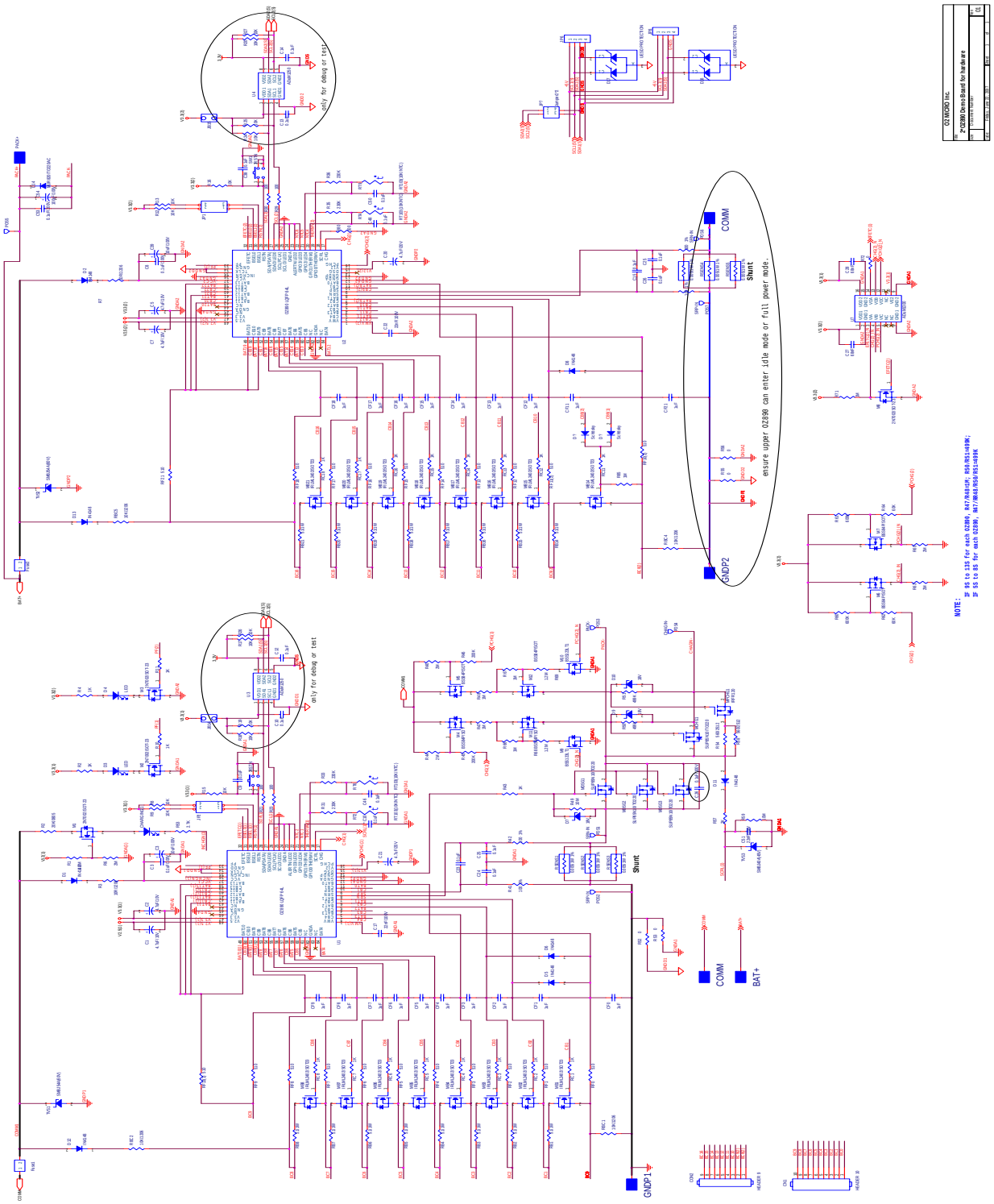


Figure2, the application circuit for dual OZ890 system (hardware mode).



As shown in Figure 2, the bottom OZ890 monitors 9 cell series of the Li-ion battery and upper OZ890 monitors 8 cells. This configuration means that cell 9 will be monitored by each OZ890. This arrangement allows cell balancing across all 16 cells connected to the two OZ890 chips. Each OZ890 works in hardware mode. This system supports the following functions:

- **Voltage measurement**
- **Temperature measurement**
- **Current measurement**
- **Balance function**
- **Protection control**
- **I^2C communication**
- **I^2C Address Configuration**

Voltage Measurement

In the system OZ890 U1 measures 9 cells' voltage (cell 1 to cell 9); and OZ890 U2 monitors 8 cells' voltage (cell 9 to cell 16). So cell 9's voltage needs to be monitored by each OZ890. This implementation achieves cell balancing across all 16 cells. This is shown in Figure 1 and in the Figure 2 schematics.

Temperature Measurement

Each OZ890 has embedded an internal temperature sensor that is for internal temperature measurement. There are 2 channels (GPIO1, GPIO2) that can be configured for external temperature measurement in hardware mode.

Please refer to figure 2.

Current Measurement

OZ890 chip's ADC current channel is a dedicated channel to measure current across the sense resistor (0.1mΩ to 15.5mΩ) during charging and discharging for coulomb counting or other purpose.

Resolution: 16-bit (signed)
Input Voltage Range: ±250mV
Auto offset cancellation

Each OZ890 needs to monitor the system current, because each OZ890 can exchange its mode (full power mode and idle mode) according to its measured current.

Please refer to figure 2.

Balance Function

In the system, each OZ890 can do cell balancing if it meets the following conditions in hardware mode:

• Battery pack is in charge state (current larger than charge current threshold) or in idle state (current smaller than charge current threshold and larger than discharge current threshold) if idle bleeding is enabled by setting bit 7 in EEPROM register 2dh.

• The bleeding function is enabled

• The highest cell voltage exceeds the BleedStartPoint voltage

• The cell voltages' difference exceeds the BleedAccuracy

• No error event, like OT, UT, OV, UV, OC, SC has occurred. If any error event happens, bleeding stops right away.

The two OZ890 chips are connected to the battery cells in a specific way in order to make cell1-cell8 have relations to cell9-cell16, and keep voltage balance among all battery cells. Each OZ890 monitors the cell 9 voltage, and in bottom OZ890 (U1) cell 1-8 compare with cell 9; and upper OZ890 (U2) cell 9-16 also compare with cell 9, so by keeping cell 9 common between the two OZ890 chips, all 16 cells achieve balance.

Protection Control

a) Discharge Mosfet control

Discharge Mosfet logic needs to be controlled by the two built-in OZ890 BPE (battery protection engine) state machines. Once one OZ890 detects any protection event, discharge mosfet should be disabled. For circuit details refer to figure 2.
Note: Upper OZ890 (U2) EFETC pin should output the discharge control logic, EEPROM register 27h Bit1-Bit0 should be set to 11. Bottom OZ890 (U1) EFETC pin should input U2's discharge logic, its EEPROM register 27 Bit1-Bit0 should be set to 01.

b) Charge/Precharge control

Charge/Precharge Mosfet logic needs to be controlled by the two built-in OZ890 BPE (battery protection engine) state machines. Once one OZ890 detects any protection event, charge/precharge mosfet should be disabled. For circuit details refer to figure 2.

I2C Communication Bus

In dual OZ890 system OZ890 works in hardware mode, only 2-wire I2C Bus is active (4-wire I2C Bus is active in software mode) but the two chips have non-common ground, therefore, I2C Bus needs to be isolated. For circuit details refer to figure 2.
In this case, BSEL0 &BSEL1 all are connected to ground.

I2C Address Configuration

For I2C communication to work properly, each OZ890 is assigned a unique I2C address. These can be set in the OZ890 EEPROM register 30h Bits (3:0).

OZ890 EEPROM register 30h:

Address	Bit3	Bit2	Bit1	Bit0
30h	I2C Addr3	I2C Addr2	I2C Addr1	I2C Addr0

Bit3 – Bit0 (I2C Addr3 – I2C Addr0): Configure the I2C address.
The I2C address = 60h (7 bits) +2N (N: 0~15).